

Inventor: Don Carl Powell

Title: Selective Oxidation Methods and Transistor Fabrication Methods

Assignee: Micron Technology, Inc.

**INFORMATION DISCLOSURE STATEMENT**

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR § 1.56. Copies of the cited art are included. No admission is made regarding whether all the submitted references are prior art.

Respectfully submitted,

Dated: 10-17-03

Attorney:   
Mark S. Matkin  
Reg. No. 32,268

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2157		SERIAL NO. Unknown	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT: Don Carl Powell			
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U.S. PATENT DOCUMENTS							
*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
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FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AJ							
	AK							
	AL							

  

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
	AM		Nagahama et al., <i>Wet Hydrogen Oxidation System for Metal gate LSI's</i> (pre-February 2001).
	AN		Ohnishi et al., <i>Improving gate oxide integrity (GOI) of a W/WNx/dual-poly Si stacked-gate by using Wet-Hydrogen oxidation in 0.14-<math>\mu</math>m CMOS devices</i> , IEEE 397-400 (September 1998).
	AO		Wakabayashi et al., <i>An Ultra-Low Resistance and Thermal Stable W/pn-Poly-Si Gate CMOS Technology using Si/TiN Buffer Layer</i> , IEEE 393-396 (September 1998).
EXAMINER		DATE CONSIDERED	

  

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS							
*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,739,066	04/14/98	Pan			
	AB	6,114,735	09/05/00	Batra et al.			
	AC	6,335,254 B1	01/01/02	Trivedi			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

  

FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AJ							
	AK							
	AL							

  

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
	AM		Hiura et al., <i>Integration Technology of Polymetal (WWSiN/Poly-Si) Dual Gate CMOS for 1 Gbit DRAMs</i>
			<i>and Beyond</i> , IEEE 398-392 (September 1998).
	AN		Kawada et al., <i>Water Vapor Generator by Catalytic Reactor</i> (pre-February 2001).
	AO		Lee et al., <i>In-situ Barrier Formation for High Reliable W/barrier/poly-Si Gate Using Denudation of WN<sub>x</sub> on</i>
			<i>Polycrystalline Si</i> , IEEE 385-388 (September 1998).
EXAMINER		DATE CONSIDERED	

  

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